POTENTIAL ANALYSIS OF A SOI MOSFET USING HIGH DIELECTRIC GATE MATERIAL

Suman Basu[1], Tiya DeyMalakar Sarkar [1], Samir Kumar Sarkar[1], Subir Kumar Sarkar[1], Nurul Islam[2]

[1]Dept of Electronics & Telecommunication Engineering, Jadavpur University, West Bengal, India
[2]Department of Mathematics, Ramakrishna Mission Residential College, Narendrapur, West Bengal, India
Email: [1]suman_basu05@rediffmail.com

Abstract

In this research work we have modeled a single gate SOI MOSFET using high dielectric gate material HfO_2 instead of as usual low dielectric gate material SiO_2. Dielectric constant of SiO_2 is 3.9 whereas HfO_2 has a value of 26 which is almost seven times (exactly 6.67) on comparison to SiO_2 gate material. Also the energy gap of HfO_2 is 5.65 eV. We have considered a long channel SOI MOSFET and Poisson's equation is solved carefully along the depth of the channel. The gradual channel approximation (GCA) technique has been considered for solving the 1-D Poisson's equation. Dependency of the surface potential with the gate biases is shown mathematically in our paper. Beside this insulating layer of HfO_2 shows several beneficial advantages like— (i) lowering the leakage current, (ii) lowering the threshold voltage and (iii) ideal sub threshold behavior.

Key words: SOI MOSFET, High K, Gradual Channel Approximation (GCA), 1-D Poisson's Equation, Surface Potential, Threshold Voltage

I. INTRODUCTION

Since 1960 Moore's law governs the semiconductor industry in VLSI chip engineering [1]. Exponential behavior of transistor technology was projected by the semiconductor industry for future implementation and this projection is the 1999 International Technology Roadmap for Semiconductors (ITRS 1999) [2]. The end of Moore's law has been predicted by H. Iwai in the last two decades without any success [3] in 2004; though some optimistic suggestions by H. Iwai [3] showed that valid Moore's law will be applicable upto 2035 and then dimension will reduce down to 0.3 nm i.e. the atomic distance between two silicon atoms in the crystal structure.

Continuous downscaling of the device dimension in the nano realm is attacked by severe short channel effects (SCEs) [4]-[5]. Silicon-on-insulator (SOI) technology is considered as a solution of appearing deleterious SCEs due to its thin channel region [5]-[8]. Further downscaling below 50 nm regime is possible as reported in [8]-[9]. Now-a-days conventional bulk MOSFET has been replaced by nanoscale SOI MOSFET for VLSI and high frequency CMOS application. Nanoscale SOI CMOS not only reduce the SCEs but also lowers the power delay product. Enhancement of the power delay product with the scaling down of dimension has been described by Shahidi [10]. Recent applications of SOI microprocessors [10]-[11] revealed the 20% speed augmentation on comparison to bulk SOI technology. Also the high power efficient SOI RF power amplifier has been reported in [12].

Various methods have been developed by the researchers for the reduction of the SCEs [13]-[14]; such as to form the ultra shallow extended source-drain junctions as reported in [15]. It is not only difficult to fabricate such type of shallow junctions by the conventional techniques but also some constraints still remain in the model [16]-[21]. To overcome the difficulties due to SCEs some researchers used dual-material gate (DMG) MOSFET structure as reported in [22]; but it is a challenging task for SOI MOSFET.

Several deleterious SCEs turn up as soon as the device dimension goes down below 100 nm and at the same time the uses of thin gate oxide faces so many problems like—direct tunneling, gate depletion and boron implantation [23]. Appearing problems due to the thin gate oxide can be much more avoided by high K dielectric material. In our present study we have taken HfO_2 as a gate material instead of as usual SiO_2 since HfO_2 is thermodynamically stable with silicon [24-26]. 1-D Poisson's equation is taken in the channel and solved it after taking the relevant boundary conditions and generalized potential profile along the depth of the

channel is studied using HfO_2 gate material. Also the off-state leakage current is much more reduced in case of HfO_2 gate material on comparison to as usual SiO_2 gate material. The K value of HfO_2 is 26 and having energy gap of 5.65 eV.

II. MODEL

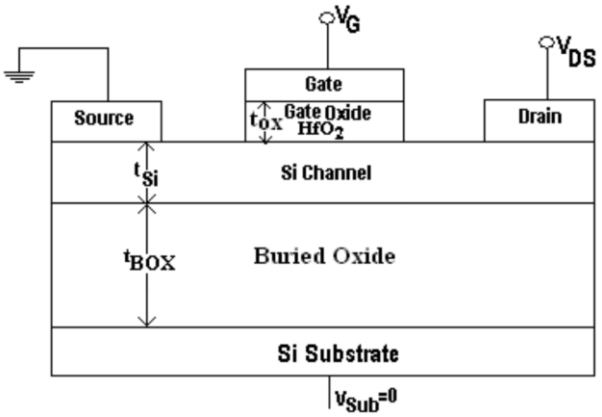

Fig.1. Cross sectional view of SOI MOSFET

The cross-sectional view of SOI MOSFET is pictured in Fig.1. In our present study we have taken an n^+ poly-silicon gate whereas channel is made by silicon material. HfO_2 is taken as an oxide material.

We have considered a long channel SOI MOSFETand from the theory of MOS devices we know that the second order differentiation of potential with respect to the horizontal axis can be ignored due to the gradual channel approximation (GCA) technique. Hence, the reduced Poisson's equation takes the shape as follows,

$$\frac{d^2\psi}{dr^2} = \frac{qn_1}{\varepsilon_{si}} e^{s(\psi - v)} \quad \text{... (1)}$$

where, q is the electronic charge, n_i is the intrinsic carrier concentration, ε_{Si} is the permittivity of Silicon, β is the inverse thermal voltage, V is the quasi-Fermi potential and channel potential is denoted ψ.

To solve the 1-D Poisson's equation we shall consider Gauss' laws at two interfaces—(a) $Si - HfO_2$ interface and (b) Si-Buried Oxide interface.

Using Gauss' law at $Si - HfO_2$ interface and we get,

$$\left.\frac{d\psi}{dy}\right|_{y=\frac{t_{ji}}{2}} = \frac{C_{OX}\,HfO_2}{z_{si}}(\psi_{si} - HfO_2 - V_{gs}) \quad \text{... (2)}$$

Similarly using Gauss' law at Si-Buried Oxide interface we get,

$$-\left.\frac{d\psi}{dy}\right|_{y=\frac{t_{ji}}{2}} = \frac{C_{3ox}}{z_{si}}\psi\, si - ROX \quad \text{... (3)}$$

In equations (2) and (3) C_{OX}, HfO_2, C_{BOX}, V_{gs} are the gate oxide capacitance and is defined by ε_{OX}, HfO_2/t_{HfO_2}, buried oxide capacitance and is defined by $\varepsilon_{BOX}/t_{BOX}$, gate voltage respectively. Permittivity of HfO_2 and thickness of the gate oxide are denoted by $\varepsilon_{ox,}$ HfO_2 and $t_{ox,\,HfO2}$ respectively. Permittivity of the buried oxide and thickness of the buried layer are denoted by ε_{BOX} and t_{BOX} respectively. Actually the gate voltage is the difference between applied gate voltage and work function difference of the gate and it is mathematically expressed as follows—

$$V_{gs,\,actual} = V_{gs,\,applied} - \phi_{MS} \quad \text{... (4)}$$

where, ϕ_{MS} = Metal semiconductor work function difference.

In our structure the depth of the channel is chosen in such a manner that $y = -t_{Si}/2$ at the uppermost point of the channel and $y = +t_{Si}/2$ at the lowermost point of the channel i.e. middle point of the channel is taken as an origin.

Integrating the Poisson's equation and taking the Gauss' law at the first interface we get,

$$\left.\int_{\frac{d\psi}{dy}}^{\frac{d\psi}{dy}} \left(\frac{dv}{dy}\right) d\left(\frac{dv}{dy}\right)\right|_{y=-\frac{t_{ji}}{2}} = \frac{qn\,\varepsilon^{-dv}}{t_{ji}} \int_{v(-t_{ji})}^{v} e^{(\beta v)\,d\psi} \quad \text{... (5)}$$

$$\frac{d\psi}{dy} = \pm\sqrt{Ae^{\beta\psi} + T_1} \quad \text{... (6)}$$

where $A = 2qn_i\, e^{(-\alpha V)/\beta\,\varepsilon_{Si}}$

and $T_1 = \left\{ \frac{d\psi}{dy} \Big| \text{at } y = -\frac{t_{si}}{2} \right\}^2 - Ae^{\beta \psi_1}$

Again integrating the Poisson's equation and taking the Gauss' law at the second interface we get,

$$\sum_{\frac{d\psi}{dy}}^{\frac{d\psi}{dy}} \Bigg|_{y=\frac{t_{ji}}{2}} \left(\frac{d\psi}{dy}\right) d\left(\frac{d\psi}{dy}\right) =$$

$$\frac{qn_i e^{-\beta V}}{\varepsilon_{si}} \int_{\psi}^{\psi} \left(-\frac{t_{ji}}{2}\right) e^{(3\psi)\, d\psi} \quad \text{... (7)}$$

$$\frac{d\psi}{dy} = \pm \sqrt{Ae^{\beta \psi} + T_2} \quad \text{... (8)}$$

where $T_2 = \left\{ \frac{d\psi}{dy} \Big| \text{at } y = +\frac{t_{si}}{2} \right\}^2 - Ae^{\beta \psi_2}$

From equation (1) we see that $\frac{d^2\psi}{dy^2}$ is always positive and with the help of theory of calculus we can conclude that solution of equation (1) does not have maxima inside the domain but having only minima. Again we are assuming that the sign of the electric field does not alter at the $Si - HfO_2$ interface and gate voltage pre-dominates the second interface potential and hence $\frac{d\psi}{dy}$ will be negative. Taking the negative sign of equation (6) we get

$$\int \frac{d\psi}{\sqrt{Ae^{\beta\psi} + T_1}} = -\int d\psi$$

$$\psi = -\frac{2}{S} \ln\left[\sqrt{\frac{A}{T_1}} \sin b\left(\frac{Q}{2}\right) \right] \quad \text{... (9)}$$

where ... (10)

$$Q = -\beta\sqrt{T_1}\left(y + \frac{t_{ji}}{2}\right) - \ln\left(\frac{\sqrt{Ae^{\beta\psi_1} + T_1} + \sqrt{T_1}}{\sqrt{Ae^{\beta\psi_1} - T_1} - \sqrt{T_1}}\right)$$

From equations (9) and (10) we see that $\sqrt{T_1}$ represents real number for $T_1 > 0$ and imaginary number for $T_1 < 0$.

Hence for $T_1 > 0$ we can write,

$$\psi(y) = -\frac{2}{S} \ln\left[\sqrt{\frac{A}{T_1}} \sin h\left\{ \frac{-S\sqrt{T_1}}{2}\left(y + \frac{T_{ji}}{2}\right) - \frac{1}{2}\ln\left(\frac{\sqrt{Ae^{\beta\psi_1} + T_1} - \sqrt{T_1}}{\sqrt{Ae^{\beta\psi_1}} - \sqrt{T_1}}\right)\right\}\right] \quad \text{... (11)}$$

And for $T_1 < 0$ we get,

$$\psi(y) = -\frac{2}{\beta} \ln\left[\sqrt{\frac{A}{T_1'}} \sin h\left\{ \frac{-\beta\sqrt{T_1'}}{2}\left(y + \frac{t_{ji}}{2}\right) - \frac{1}{2}\ln\left(\frac{\sqrt{Ae^{\beta\psi_1} + T_1} - \sqrt{T_1}}{\sqrt{Ae^{\beta\psi_1}} - \sqrt{T_1}}\right)\right\}\right] \quad \text{... (12)}$$

Equations (11) and (12) represent the two shapes of potential profiles along the thickness of the channel. Nature of the potential profile depends on the gate voltage. In the above mentioned two equations one term is unknown— $\psi_{Si-HfO2}$. Now applying equation (3) to equations (11) and (12) we get two implicit equations as follows respectively,

$$\theta = \sin h - \left[\frac{1}{\sqrt{p_1}} e^{(-\beta\, \varepsilon_{si}\sqrt{T_2}/2\, C_{BOX})/(-i \tan(i\theta))} \right] \quad \text{... (13)}$$

$$\theta^* = \sin^{-1}\left[\frac{1}{\sqrt{P_1^*}} e^{\frac{-\sqrt{}\,\beta_{si} \cot(\theta^*)}{T_2^* C_{BOX}}} \right] \quad \text{... (14)}$$

where

$$\theta = \beta(\sqrt{T_1}\, t_{si}/2) + \sinh^{-1}(e^{-S\psi_1/2}/\sqrt{F_1})$$

$$\theta^0 = \beta\left(\sqrt{T^0}\, 1^t \pi/2\right) + \sin^{-1}\left(e^{-\beta\psi_1/2}/\sqrt{p_1^0}\right)$$

$$t = \sqrt{-1}$$

$$P_1 = \frac{A}{T_1}$$

$$P_1^0 = -P_1$$

$$T_1^* = -T_1$$

So we have to take either equation (11) or equation (12). To find out the complete solution of equation (11) or equation (12) we have to solve equations (13) or (14) for getting the potential profile. Actually the potential profile depends on the sign of the

T; here we can say that Tzero point is a most significant term to get the final solution. T zero point (TZP) can be defined on a manner that it is the point where T becomes zero. Equating T_1 to zero we get one solution of sub tzp and it is derived as follows

$$\psi_{cap} = V_{gs} - \frac{2}{s} W\left\{ \frac{S}{2^0}\left(\frac{\beta V_{as}}{2}\right)\sqrt{\frac{A\varepsilon_{si}^2}{C_{ox}^2(sio_2/HfO_2)}} \right\} \quad \ldots (15)$$

where W represents the Lambert's function.

III. RESULTS AND DISCUSSION

Variation of T_1 with first interface potential ψ_1 is shown in Fig. 2 for two gate voltages. From the graphs we can explain the definition of T zero point; where the graphs cut the zero line. Curve shifts upward with the increment of the gate voltages. We have to choose equations (11) or (12) depending on the position of the point on the graph i.e. whether it (the point) lies above the zero line (positive value) or below the zero line (negative value). First interface potential ψ_1 can be obtained from equations (13) and (14).

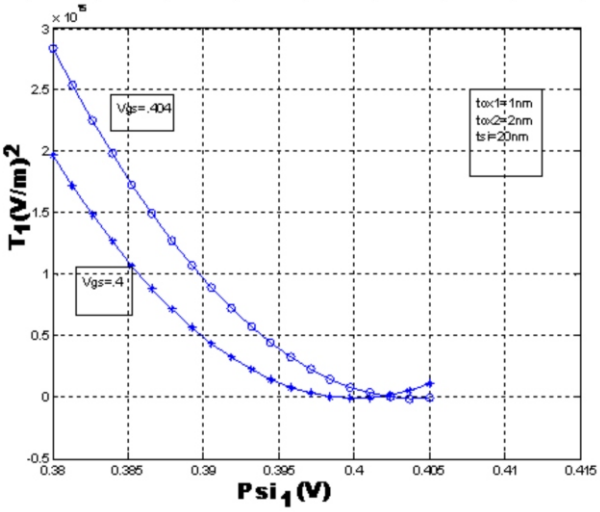

Fig. 2 Variation of T zero point with interface potential ψ_1 taking two gate voltages $V_{gs} = 0.4$ V (Left) and 0.404 V taking $t_{HiO_2} = 2$ nm, $t_{BOX} = 100$ nm and $t_{Si} = 20$ nm for HfO_2

Variation of the potential profile with the depth of the channel has been studied in Fig.3. It is observed that the potential profile decays with the depth of the channel. Gate voltage has been taken the constant value of 0.4 V. Nature of the potential profile can be elucidated with the help of equation (11); since sqrt. (P_1) and sqrt. (T_1) both are positive so ψ decreases with thickness when thickness of the channel increases towards the positive direction.

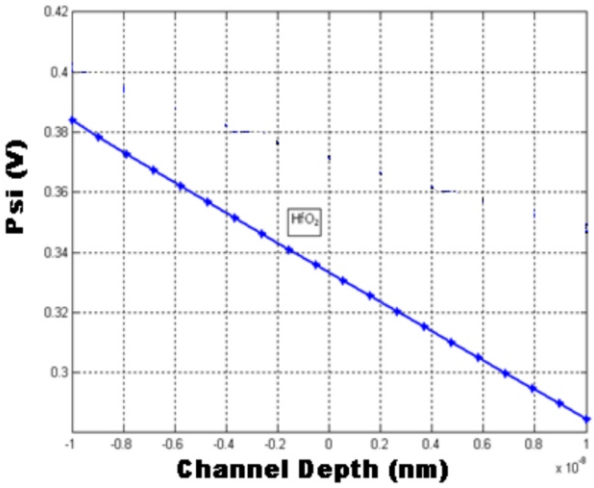

Fig. 3 Variation of potential profile with the depth of the channel, taking gate voltage $V_{gs} = 0.4$ V, taking $t_{HfO_2} = 2$ nm, $t_{BOX} = 100$ nm and $t_{Si} = 20$ nm for SiO_2/HfO_2

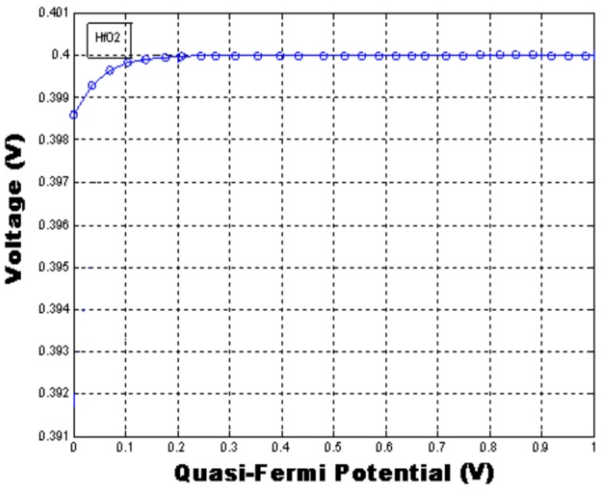

Fig. 4 Variation of ψ_{tzp} with quasi-Fermi potential

Variation of ψ_{tzp} with quasi-Fermi potential is shown in Fig. 4. Since ψ_{tzp} saturates at high value of quasi-Fermi potential, so we have taken the smallest variation along the y-axis i.e. along the sub ψ_{tzp}. Typical nature of the graph can be explained with the help of equation (14); since ψ_{tzp} varies with the

square root of A so ψ_{tzp} saturates at high values of quasi Fermi potential.

IV. CONCLUSION

An analytical model of long channel SOI MOSFET is thoroughly studied in our paper. Potential profile along the depth of the channel is analyzed and it's with the gate biases is described with the mathematical function, i.e. (y). Ultimately we have reached a general solution of 1-D Poisson's equation for single gate SOI MOSFET. The mathematics of the model for long channel independent double gate MOSFET was described by A. Sahoo et. al. [27] but in this work we have considered a single gate SOI MOSFET. Also the role of high K dielectric HfO_2 is shown in our model.

REFERENCES

[1] Bondy P.K., Jan. 1998,Moore's law governs the silicon revolution, Proc. IEEE, 86, pp. 78-81..

[2] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors, 1999 ed. San Jose, CA: SIA, 1999.

[3] Iwai H., Dec 2004, Future semiconductor manufacturing: Challenges and Opportunities, in IEDM Tech. Dig., pp. 11-16.

[4] Frank D.J., Dennard R.H., Nowak E., Solomon P.M., Taur Y. and Wong H.-S., March 2001,.Device scaling limits of Si MOSFETs and their application dependencies, Proc. IEEE, 89(3), pp. 259-288.

[5] Boyle B., Arghavani R., Barlage D., Datta S., Doczy M., Kavalieros J., Murthy A., and Chau R., May 2002, Transistor elements for 30 nm physical gate lengths and beyond, Intel Technol. J*, vol. 6(2), pp. 42-54. http://developer.intel.com/technology/itj./*

[6] Cristoloveanu S. and Ferlet-Cavrois V., Jun. 2004, Introduction to SOI MOSFETs: Context, radiation effects, and future trends,Int. J. High Speed Electron. Syst., vol. 14(2), pp. 465-487,.

[7] Fossum J.G., Trivedi V.P., and Wu K. Oct. 2002, Extremely scaled fully depleted SOI CMOS, in Proc. IEEE Int. SOI Conf.,pp. 135-136.

[8] Lemnios Z.J., Radack D. J., and. Zolper J. C, Oct. 2004, The future of silicon-on-insulator (SOI) technology in microelectronic systems, in Proc. Int. SOI Conf., pp. 9-13.

[9] Colinge J.-P., Sep. 2004 ,Novel gate concepts for MOS devices, in Proc. 34th ESSDERC, pp. 45-49.

[10] Shahidi G.G. ,Mar.-May 2002.,SOI technology for the GHz era, IBM J. Res. Develop., vol. 46(2/3), pp. 121-131.

[11] Park S.B., Kim Y.W., Ko Y.G., Kim K.I., Kim I.K., Kang H.-S., Yu J.O., and Suh K.P., Nov. 1999. A 0.25 %m, 600-MHz, 1.5-V, fully depleted SOI CMOS 64-bit microprocessor, IEEE J. Solid-State Circuits,34(11), pp. 1436-1445.

[12] Fiorenza J.G. and Alamo J.A. del, Experimental comparison of RF power LDMOSFETs on thin-film SOI and bulk silicon, IEEE Trans. on Electron. Dev., 49(4), pp. 687-692.

[13] Kon R., 1999, Buried layer engineering to reduce the drain-induced barrier lowering of sub sub- 0.05 %m SOI-MOSFET, Japanese Journal of Applied Physics, 38, pp. 2249-2299.

[14] Chaudhury A. and Kumar M. J., March 2004, Controlling short-channel effect in deep-submicron SOI MOSFETs for improved reliability: A review, IEEE Trans. Dev. Mater. Reliabil., 4(3), pp. 99-109.

[15] Kumar M.J. and Orouji Ali A., July 2005, Two-dimensional analytical threshold voltage model of nanoscale fully depleted SOI MOSFET with electrically induced S/D extensions, IEEE Transactions on Electron Devices, 52(7).

[16] Kawaura H., Sakamoto T., Baba T., Ochiai Y., Fujita J., Matsui S., and Sone J., March 1998, Transistor operation of 30 nm gate-length EJ-MOSFETs, IEEE Electron Device Lett.,19(3), pp. 74-76.

[17] Han S., Chang S., Lee J. and Shin H., September 2011, 50 nm MOSFET with electrically induced source/drain (S/D) extensions, IEEE Trans. Electron Devices, 48(9), pp. 2058-2064.

[18] Xusheng W., Shendong Z., Chan M. and Chan P., 2003, Design of sub-50 nm ultrathin-Body (UTB) SOI MOSFETs with raised S/D, IEEE Conf. Electron Devices Solid-State Circuits, pp. 251-254.

[19] Hartstein A., Albert N. F.,Bright A. A., Kaplan S. B., Robinson S. B. and Tornello J.A., 1990, A metal-oxide-semiconductor field effect transistor with a 20 nm channel length, J. Appl. Phys,68, pp. 2493-2495.

[20] Wang H.S., 1991, Experimental verification of the mechanism of hot-carrier-induced photon emission in N-MOSFETs with a CCD gate structure, in IEDM Tech. Dig., pp. 549-552.

[21] Noda H., Murai F. and Kimura S., 1993, Threshold voltage controlled 0.1%m MOSFET utilizing inversion layer as extreme shallow source/drain, in IEDM Tech. Dig.,pp. 123-126.

[22] Reddy G.Venkateshwar and Kumar M. Jagadesh, 2005, A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-Two dimensional analytical modeling and simulation, IEEE Transactions on Nanotechnology, 4(2), pp. 260-268.

[23] Ahmed Monsoor M., May 2001, Schottky Barrier Depletion Modification-A Source of Output Conductance in Submicron GaAs MESFETs, IEEE Transactions on Electron Devices,48(5).

[24] Martinez F.L., Toledano-Luque M., Gandia J. J., Carabe J, Bohne W, Rohrich J, Strub E and Martil I, 2007, Optical properties and structure of HfO_2 thin films grown by high pressure reactive sputtering, Journal of Physics D: Applied Physics 40, pp.5256-5265.

[25] Kang Laegu, Onishi Katsunori, Jeon Yongjoo, Lee Byoung Hun, Kang Changseok, Qi Wen-Jie, Nieh Renee, Gopalan Sundar, Choi Rino, and Lee Jack C., MOSFET Devices with Polysilicon on Single-Layer HfO sub 2 High-K Dielectrics Microelectronics Research Center, R9950, Department of Electrical and Computer Engineering The University of Texas at Austin, Austin, Texas 78758, (512)471- 1627.

[26] Yeo Yee-Chia, King Tsu-Jae and Hu Chenming, 2003, MOSFET Gate Leakage Modeling and Selection Guide for Alternative Gate Dielectrics Based on Leakage Considerations, IEEE Trans. on Electron Devices, pp.1-9.

[27] Sahoo Avinash, Thakur Pankaj Kumar, and Mahapatra Santanu, March 2010, A computationally efficient generalized Poisson solution for independent double-gate transistors, *IEEE Transactions on Electron Devices, 57(3).*

Suman Basu was born in Kolkata, India. He received his B.Sc. (Hons.) and M.Sc. in Electronic Science in 2004 and 2006 respectively. Presently he is pursuing his Ph.D. research in Jadavpur University in the department of Electronics & Telecommunication Engineering. His current research focuses on advanced MOS device, micro and nano devices.

Nurul Islam received B.Sc (Hons.) and M.Sc. in Mathematics from University of Calcutta. He completed his Ph.D in Mathematics from Jadavpur University. Presently he is an Associate Professor and Head of the Department of Mathematics in Ramakrishna Mission Residential College, Narendrapur.

Samir Kumar Sarkar received B.Tech., M. Tech. and Ph.D. (Tech.) from Jadavpur University. Presently he is a faculty of Jadavpur University in the department of Electronics and Telecommunication Engineering. Presently he is guiding four Ph.D. students under his supervision. His research work focuses on SOI, DG MOSFET and SON MOSFET.

Subir Kumar Sarkar received the B.Tech and M.Tech Degree and Ph.D.(Tech) from the Institute of Radio Physics and Electronics, University of Calcutta. He was in Industry for ten years and presently a Professor in the Department of Electronics & Telecommunication Engineering, Jadavpur Universty. He has in his credit more than 300 research papers published in International/National journals and conference proceedings. He has published three engineering text books and 25 students have been awarded Ph.D. degree under his guidance. His most recent research focus is in the areas of simulations of SOI/SON MOSFET, nanodevice models, transport phenomenon, single electron & spintronics devices and their applications in VLSI circuits, low power VLSI design. He is a life Fellow of the Institution of Engineers and Institution of Electronics and Telecommunication Engineers, life member of ISTE, life member of Indian Asociation for the cultivation of Science, Senior member of IEEE.